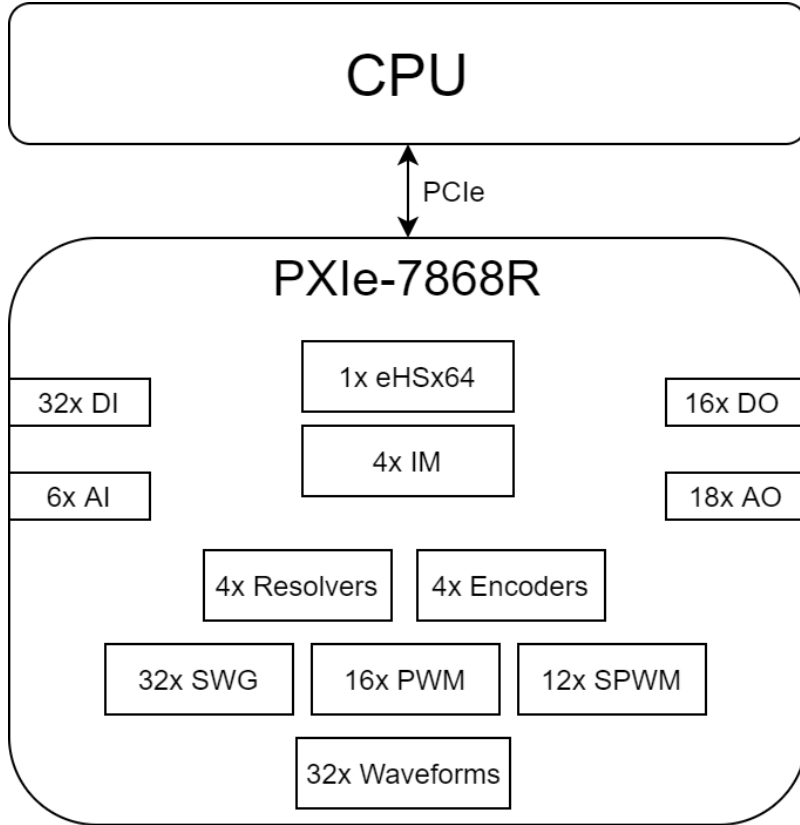


eHSx64_Quad_IM_SM_IO_7868R

Specifications



IO Capabilities

This configuration requires the following FPGA boards. Please refer to the linked product page for additional information.

Quantity	FPGA Board
1	PXIe-7868R

The PXIe-7868R supports the following features:

IO Type	Details
Analog Input	6 CH, 1MS/s, 16-bit, +/- 10V Input Signal Range, Differential Tunable Gain, Offset, and Min/Max Saturation
Analog Output	18 CH, 1MS/s, 16-bit User-defined mapping to Analog Outputs available with tunable Gain, Offset, and Min/Max Saturation. <ul style="list-style-type: none"> • Measurements • Sinewaves • CPU (VeriStand) • Machines
Digital Input	32 CH, 80MHz, 3.3V TTL (Connector 1)

Digital Output	<p>16, 10MHz, 3.3V TTL (Connector 0)</p> <p>User-defined mapping to Digital Outputs available with tunable Polarity.</p> <ul style="list-style-type: none"> • CPU (VeriStand) • Encoders • PWMs • Digital Inputs
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Refer to [7868 IO Assignment \[eHSx64_Quad_IM_SM_IO_7868R\]](#) to see the IO assignment.

Modeling Capabilities

This configuration includes a pre-compiled firmware/bitfile which contains the following features:

Features	Additional Information
1x eHSx64 Solver	<p>User-defined mapping to Circuit Sources available:</p> <ul style="list-style-type: none"> • CPU (VeriStand) • Sinewaves • Machines • Analog Inputs <p>User-defined mapping to Circuit Switches available:</p> <ul style="list-style-type: none"> • CPU (VeriStand) • PWMs • SPWMs • Digital Inputs
4x Squirrel-Cage Induction Machine Solver	Refer to the SCIM Model Description for more information
1x Resolver/motor	Excitation is assignable to any Analog Input port.
1x Encoder/motor	Outputs are assignable to any Digital Output port.
32x Sinewave Generators	
16x PWM Generators	
12x Sinusoidal PWM Generators	
Analog Output Mapping and Rescaling	
Analog Input Rescaling	
32x Waveform Acquisition Channels	