# 4.8 Configuring the Local Controller

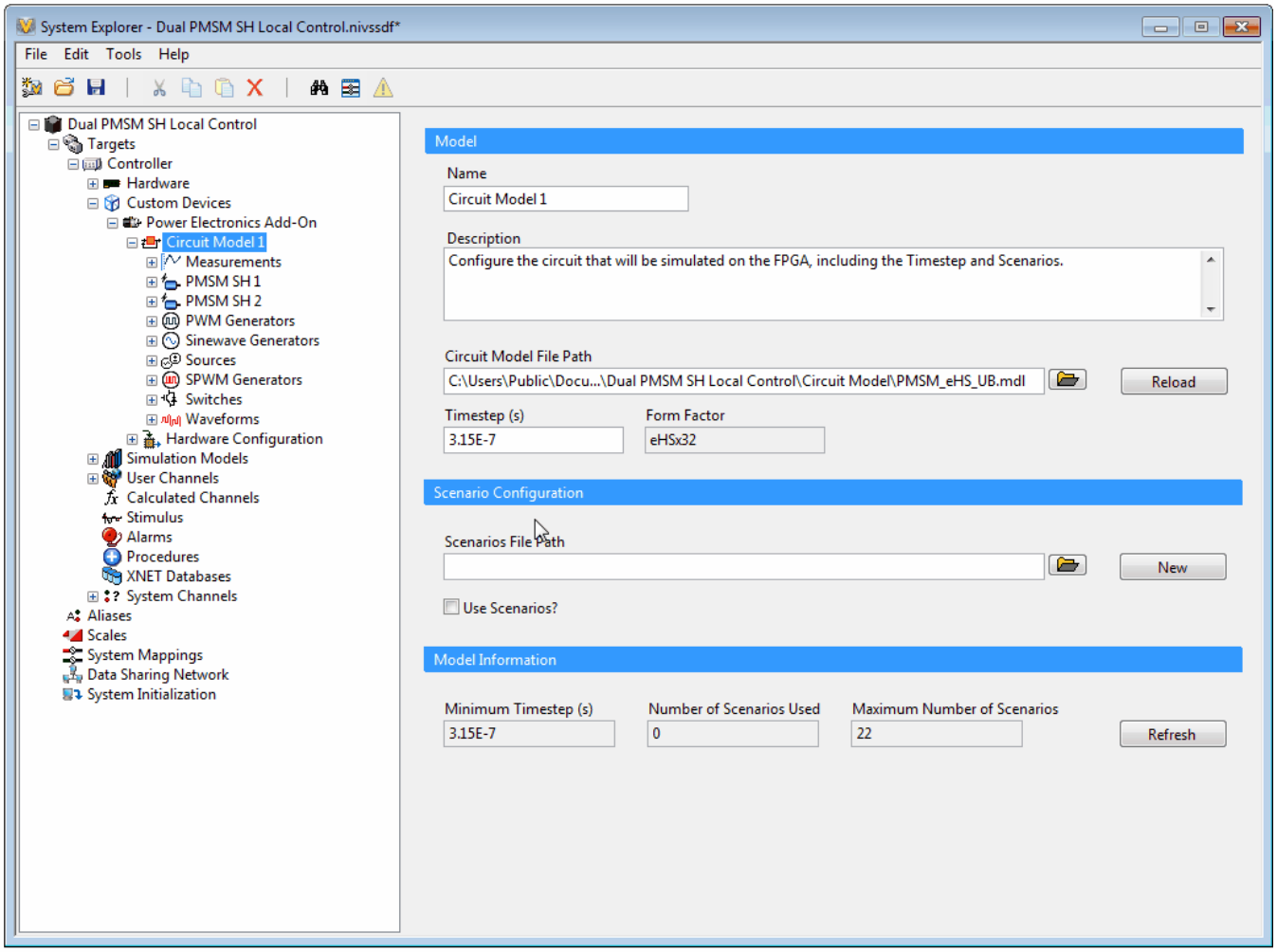
A simple closed-loop SPWM frequency and modulation index controller model was developed for this example. It has been compiled into *.dll* and *.so* files for execution on both Phar Lap and Linux RT targets, respectively. The controller model is configured to run on the Real Time CPU and will be executed by the **VeriStand Engine**. Data is routed from the CPU simulation (local controller) to the FPGA simulation (eHS, SCIM model) using the VeriStand System Configuration Mappings.

**Local Controller File Path**: *<Public Documents>\National Instruments\<NI VeriStand 20xx>\Examples\OPAL-RT\Power Electronics Add-On\Dual PMSM SH Local Control\Local Controller\VoltPerHertzController*

## Exploring the Local Controller

- In the Configuration Tree, expand **Controller >> Simulation Models >> Models**. Click **Volts Per Hertz Controller** to view the model file information.
- By default, the *.so* file is loaded for execution on a **Linux RT** target. To run the example on a **Phar Lap** target, click the **Browse Simulation Model** button in the Menu bar and select *VoltPerHertzController.dll* from the **Local Controller File Path** listed above.
- In the Configuration Tree, expand **Volt Per Hertz Controller >> Inports** and confirm that all inports have been configured as shown in the table below.
- Click **Save.**

| Inport | Default Value |
|---|---|
| **Dclink** | 0 |
| **DesiredSpeedRPM** | 0 |
| **ModIndexLookup** | 0 0.001<br>120 6<br>240 12<br>480 25<br>720 38<br>1200 62<br>1800 92<br>2000 100<br>2400 122<br>3000 150 |
| **Poles** | 5 |
| **RampRate** | 10 |

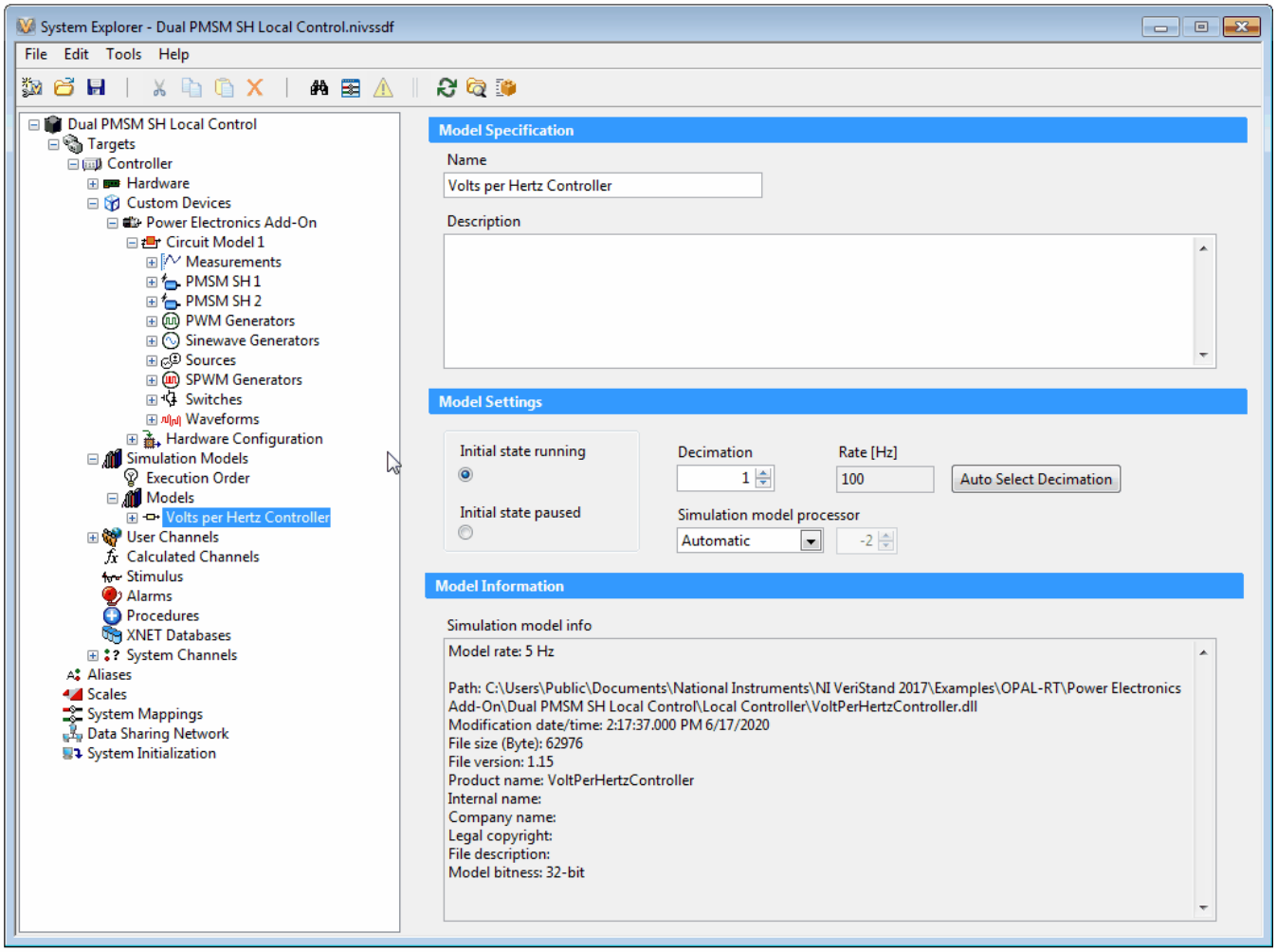



## Exploring the Mappings to and from the Local Controller

The VeriStand System Configuration Mappings are used to route signals between the local controller and the other model components simulated on the FPGA.

- In the VeriStand System Explorer window, navigate to **Tools >> Edit Mappings** in the Menu bar.
- Confirm that the mappings are configured as shown in the table below.

| Sources | Destinations |
|---|---|
| *Controller/User Channels/**Grid Amplitude*** | *Controller/Custom Device/OPAL-RT Power Electronics Module/Circuit Model/Signal Generators /Sinewave Generators/SWG Generator 0/**Amplitude*** |
| *Controller/User Channels/**Grid Amplitude*** | *Controller/Custom Device/OPAL-RT Power Electronics Module/Circuit Model/Signal Generators /Sinewave Generators/SWG Generator 1/**Amplitude*** |
| *Controller/User Channels/**Grid Amplitude*** | *Controller/Custom Device/OPAL-RT Power Electronics Module/Circuit Model/Signal Generators /Sinewave Generators/SWG Generator 2/**Amplitude*** |
| *Controller/Simulation Models/Models/Volts per Hertz Controller/Outports/**InverterFrequencyRef*** | *Controller/Custom Device/OPAL-RT Power Electronics Module/Circuit Model/Signal Generators /SPWM Generators/SPWM Frequency Generators/**SPWM Frequency Engine 0*** |
| *Controller/Simulation Models/Models/Volts per Hertz Controller/Outports/**ModIndexRef*** | *Controller/Custom Device/OPAL-RT Power Electronics Module/Circuit Model/Signal Generators /SPWM Generators/SPWM Carrier/**Modulation Index*** |
| *Controller/Custom Device/OPAL-RT Power Electronics Module/Circuit Model/Measurements/**Y04 Vdc*** | *Controller/Simulation Models/Models/Volts per Hertz Controller/Inports/**Dclink*** |


System Explorer - Dual PMSM SH Local Control.nivssdf
File Edit Tools Help
Dual PMSM SH Local Control
Targets
Controller
Hardware
Custom Devices
Power Electronics Add-On
Circuit Model 1
Measurements
PMSM SH 1
PMSM SH 2
PWM Generators
Sinewave Generators
Sources
SPWM Generators
Switches
Waveforms
Hardware Configuration
Simulation Models
Execution Order
Models
Volts per Hertz Controller
User Channels
Calculated Channels
Stimulus
Alarms
Procedures
XNET Databases
System Channels
Aliases
Scales
System Mappings
Data Sharing Network
System Initialization
Model Specification
Name
Volts per Hertz Controller
Description
Model Settings
Initial state running
Initial state paused
Decimation
1
Rate [Hz]
100
Auto Select Decimation
Simulation model processor
Automatic
-2
Model Information
Simulation model info
Model rate: 5 Hz
Path: C:\Users\Public\Documents\National Instruments\NI VeriStand 2017\Examples\OPAL-RT\Power Electronics Add-On\Dual PMSM SH Local Control\Local Controller\VoltPerHertzController.dll
Modification date/time: 2:17:37.000 PM 6/17/2020
File size (Byte): 62976
File version: 1.15
Product name: VoltPerHertzController
Internal name:
Company name:
Legal copyright:
File description:
Model bitness: 32-bit