5.8 Configuring the Local Controller

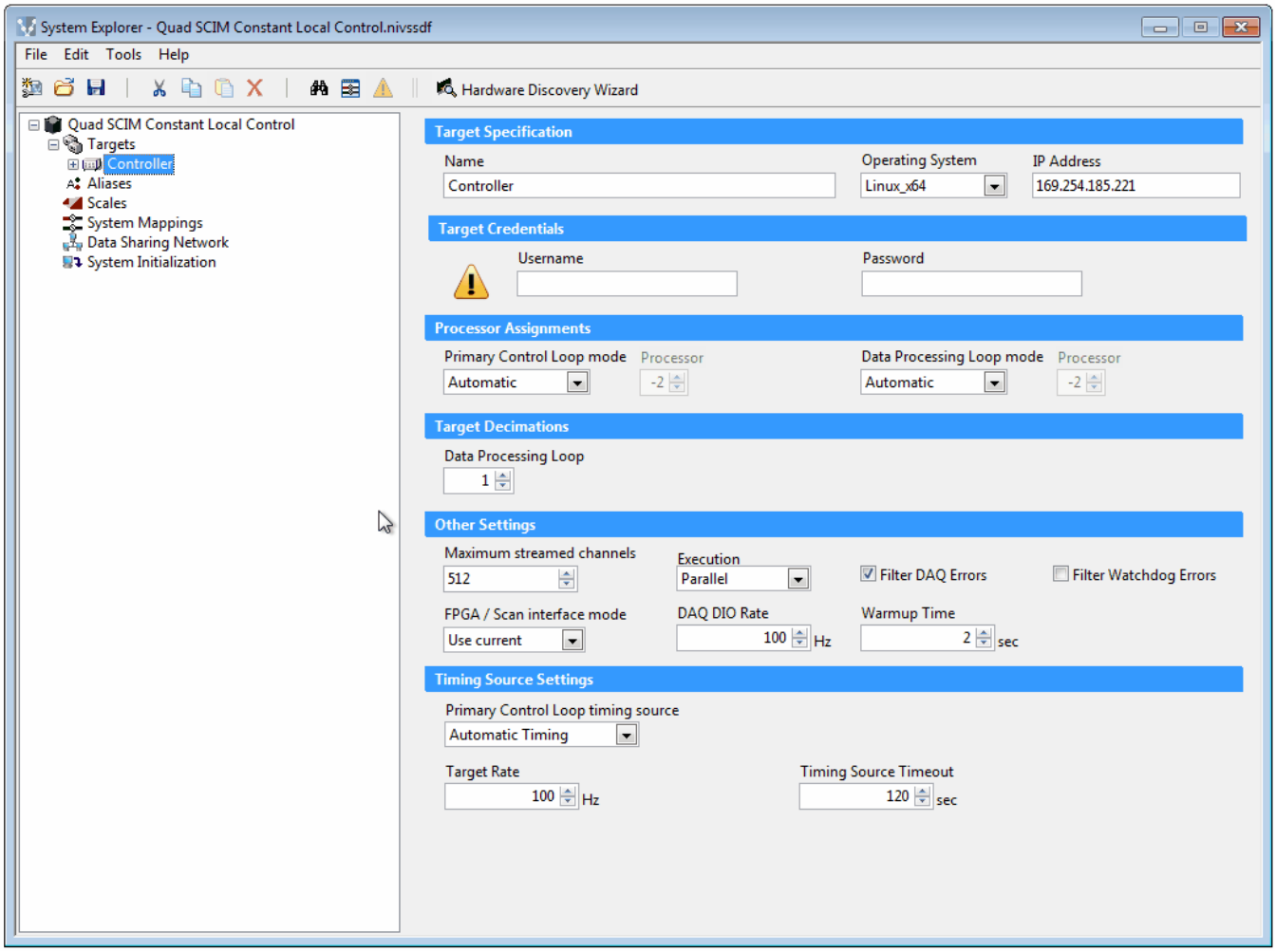
A simple closed-loop SPWM frequency and modulation index controller model was developed for this example. It has been compiled into *.dll* and *.so* files for execution on both Phar Lap and Linux RT targets, respectively. The controller model is configured to run on the Real Time CPU and will be executed by the **VeriStand Engine**. Data is routed from the CPU simulation (local controller) to the FPGA simulation (eHS, SCIM model) using the VeriStand System Configuration Mappings.

Local Controller File Path: *<Public Documents>\National Instruments\<NI VeriStand 20XX>\Examples\OPAL-RT\Power Electronics Add-On\Quad SCIM Constant Local Control\Local Controller*

Exploring the Local Controller

- In the Configuration Tree, expand **Controller >> Simulation Models >> Models**. Click **ClosedLoopVoltPerHertzController** to view the model file information.
- By default, the *.so* file is loaded for execution on a **Linux RT** target. To run the example on a **Phar Lap** target, click the **Browse Simulation Model** button in the Menu bar and select *ClosedLoopVoltPerHertzController.dll* from the **Local Controller File Path** listed above.
- In the Configuration Tree, expand **ClosedLoopVoltPerHertzController >> Inports** and confirm that all inports have been configured as shown in the table below.
- Click **Save.**

Inport	Default Value
Dclink	0
DesiredSpeedRPM	0
ModIndexLookup	1 10 100 75 500 200 1000 650 2000 830 3000 830 4000 830 5000 830 6000 830 7000 830
Poles	3
RampRate	50
SpeedRPM_I	0.001
SpeedRPM_P	0.01
SpeedRPMProcess	0



Exploring the Mappings to and from the Local Controller

The VeriStand System Configuration Mappings are used to route signals between the local controller and the other model components simulated on the FPGA.

- In the VeriStand System Explorer window, navigate to **Tools >> Edit Mappings** in the Menu bar.
- Confirm that the mappings are configured as shown in the table below.

Sources	Destinations
*Controller/User Channels/**Input Voltage Amplitude***	*Controller/Custom Device/OPAL-RT Power Electronics Module/Circuit Model/Signal Generators/Sinewave Generators/SWG 0/**Amplitude***
*Controller/User Channels/**Input Voltage Amplitude***	*Controller/Custom Device/OPAL-RT Power Electronics Module/Circuit Model/Signal Generators/Sinewave Generators/SWG 1/**Amplitude***
*Controller/User Channels/**Input Voltage Amplitude***	*Controller/Custom Device/OPAL-RT Power Electronics Module/Circuit Model/Signal Generators/Sinewave Generators/SWG 2/**Amplitude***
*Controller/Simulation Models/Models /ClosedLoopVoltPerHertzController/Outports/**InverterFrequencyRef***	*Controller/Custom Device/OPAL-RT Power Electronics Module/Circuit Model/Signal Generators/SPWM Generators/SPWM Frequency Generator/**SPWM Frequency Engine 0***
*Controller/Simulation Models/Models /ClosedLoopVoltPerHertzController/Outports/**ModIndexRef***	*Controller/Custom Device/OPAL-RT Power Electronics Module/Circuit Model/Signal Generators/SPWM Generators/SPWM Carrier/**Modulation Index***
*Controller/Custom Device/OPAL-RT Power Electronics Module/Circuit Model/Measurements/**Y04 Vdc***	*Controller/Simulation Models/Models/ClosedLoopVoltPerHertzController/Inports/**Dclink***

*Controller/Custom Device/OPAL-RT Power Electronics Module/Circuit Model/SCIM 1/Mechanical Model/**Speed***	*Controller/Simulation Models/Models/ClosedLoopVoltPerHertzController/Inports/**SpeedRPM Process***