Digital Inputs Section

Digital Inputs Configuration Page

This page is populated with a list of the Digital Input channels available for the selected **Hardware Configuration**.

The following configuration options are available:

Enable PWM Measurement Channels	Enables the PWM Measurement feature for every Digital Input channel. When this option is enabled, an **Advanced** subsection is created under the Digital Inputs section and populated with **DI*XX* Duty Cycle** and **DI*XX* Frequency** channels as described in the table below.

Digital Inputs Section Channels

This section includes the following custom device channels:

Channel Name	Type	Units	Default Value	Description
DI*XX* Duty Cycle	Output	Percent	0%	Duty Cycle of the digital signal acquired on channel *DI<XX>*. Accuracy information can be found under **PWM Measurement Accuracy**. When **Enable PWM Measurement Channels** is enabled, the **Digital Inputs >> Advanced >> Duty Cycle** section is populated with one **DI*XX* Frequency** channel for each Digital Input channel.
DI*XX* Frequency	Output	Hertz	0Hz	Frequency of the digital signal acquired on channel *DI<XX>*. Accuracy information can be found under **PWM Measurement Accuracy**. When **Enable PWM Measurement Channels** is enabled, the **Digital Inputs >> Advanced >> Frequency** section is populated with one **DI*XX* Frequency** channel for each Digital Input channel.
DI*XX*	Output		0	Digital data read by the FPGA on channel *DI<XX>*. The Digital Inputs section is populated with one **DI*XX*** channel for each Digital Input channel available in the selected **Hardware Configuration**.

Digital Input data can be mapped to other simulation components by navigating to their respective configuration pages listed below. Mapping options may vary between **Hardware Configurations**.

- Circuit Switches
- Waveforms
- Resolver Excitation

PWM Measurement Accuracy

The accuracy of the PWM Measurement feature is dependent upon the frequency and duty cycle of the measured signal. The tables below provide benchmark information describing the maximum expected measurement error across a range of PWM frequencies.

Table 1: Error in Frequency Measurement

These data points have been validated for Duty Cycles between 0.1 and 0.9.

Frequency Range	Percent Error in Frequency Measurement
1Hz - 10Hz	< 0.5%
10Hz - 100Hz	< 0.05%
100Hz - 1kHz	< 0.01%
1kHz - 10kHz	< 0.05%
10kHz - 100kHz	< 0.1%
100kHz - 500kHz	< 2%

Table 2: Error in Duty Cycle Measurement

Duty cycle error has been measured at three Duty Cycles: 0.1, 0.5, and 0.9.

Frequency Range	Percent Error in Duty Cycle Measurement Duty Cycle: 0.1	Percent Error in Duty Cycle Measurement Duty Cycle: 0.5	Percent Error in Duty Cycle Measurement Duty Cycle: 0.9
1Hz - 10Hz	< 0.0005%	Negligible	Negligible
10Hz - 100Hz	< 0.005%	< 0.001%	< 0.001%
100Hz - 1kHz	< 0.05%	< 0.01%	< 0.01%
1kHz - 10kHz	< 0.1%	< 0.05%	< 0.05%
10kHz - 100kHz	< 1%	< 0.1%	< 0.1%
100kHz - 500kHz	< 10%	< 2%	< 1%

Table 3: Minimum Detected Frequency

If a signal with a frequency below the **Minimum Detected Frequency** is applied, the corresponding VeriStand Channels will output *NaN* (Not a Number) after the **Settling Time** has elapsed.

Hardware Configuration	Minimum Detected Frequency	Settling Time
eHSx32_Dual_PMSM_SH_IO_7868R	0.5 Hz	2 s
eHSx32_Dual_PMSM_VDQ_IO_32DO_7868R	0.5 Hz	2 s
eHSx64_Dual_PMSM_VDQ_IO_7868R	0.25 Hz	4 s
eHSx64_Quad_IM_SM_IO_7868R	0.25 Hz	4 s