

How to Simulate a Drive with a Machine

Prerequisites

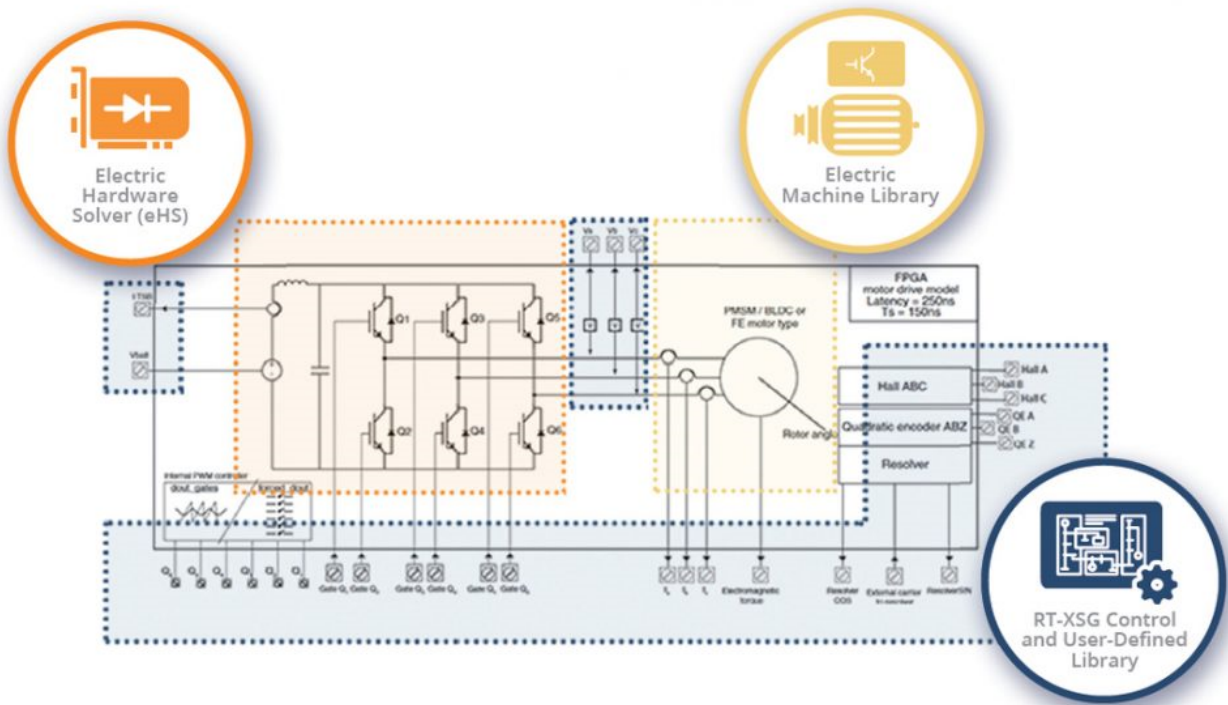
[How to Add the Power Electronics Add-On to the System Definition](#)

[How to Create a Circuit Model](#)

[How to Add a Circuit Model to the System Definition](#)

Procedure

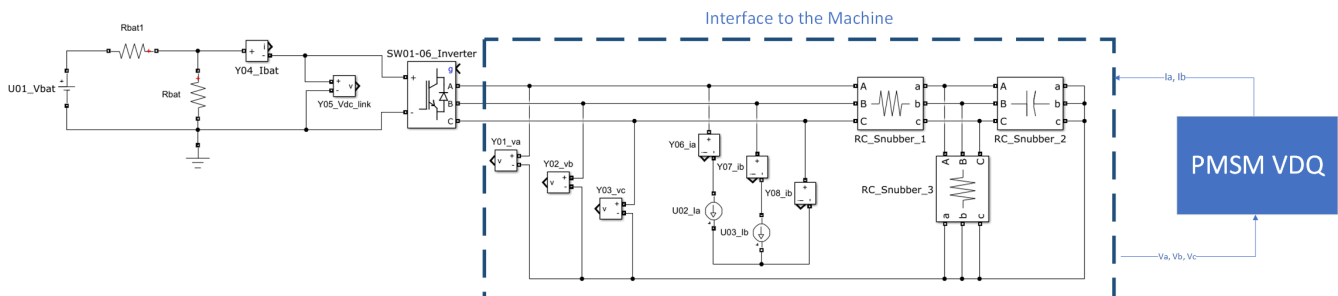
Different modeling resources within the FPGA design are used to simulate different parts of the electrical model. For example, in the case of a drive system, the circuit containing linear elements is simulated using the **eHS Solver**, whereas the machine configuration is simulated with a **Machine Model** (see image below). Due to this inherent decoupling of the two parts of the simulation, additional considerations must be made when simulating a drive coupled to a machine.



Interface Requirements to Couple a Drive and a Machine

To couple a drive circuit with a machine, such as a PMSM, a specific set of **Sources** and **Measurements** must be added to the circuit model. In the case of the PMSM, typically, it is important to include the following interface elements:

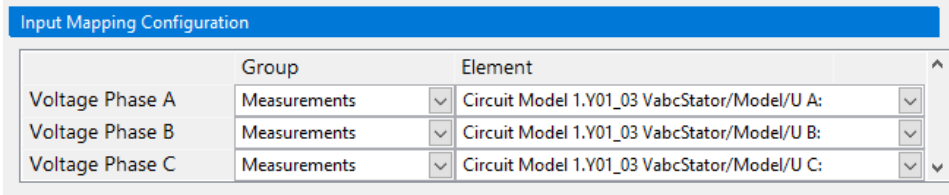
- Measurements for the three phase voltages (V_a , V_b , V_c) that will be output from the drive model (eHS) and fed into the machine model
- Sources for the currents (I_a , I_b) that will be output from the machine model and injected into the drive model (eHS)
- RC snubbers to compensate for the decoupling of the two solvers on the FPGA. Please see [Tuning the Snubber Values](#) for more information.



Configuring the Routing between the Drive and the Machine

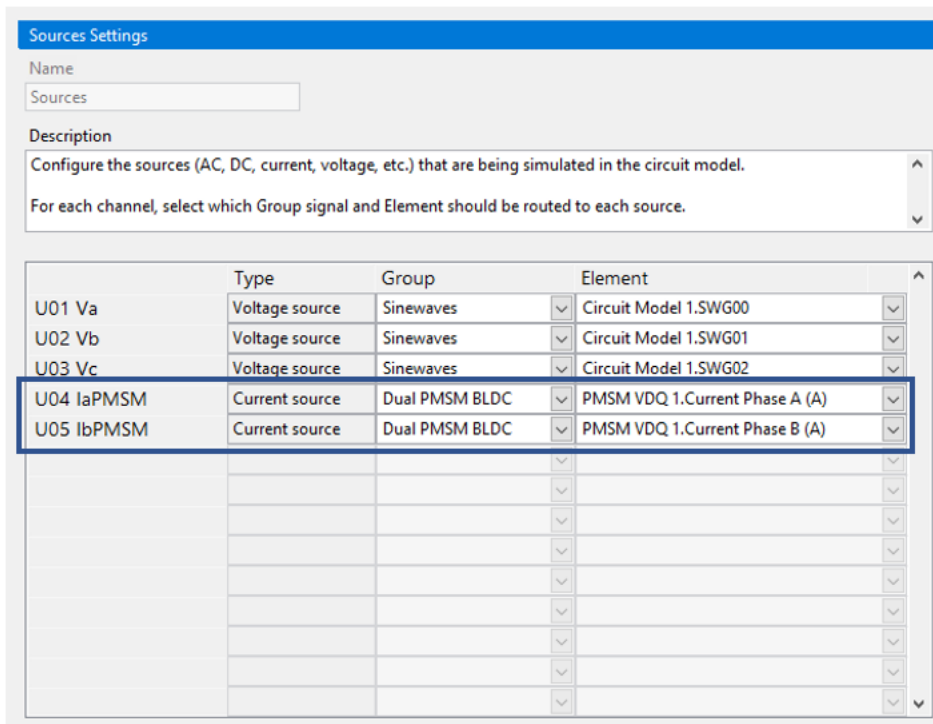
To map the interface Sources and Measurements of the circuit to the Machine Model:

1. In the VeriStand System Definition, navigate to the **Machine Model** configuration page.
2. Under **Input Mapping Configuration**, map the three voltage measurements to the **Voltage Phase A**, **Voltage Phase B**, and **Voltage Phase C** inputs of the machine model.



| | Group | Element |
|-----------------|--------------|--|
| Voltage Phase A | Measurements | Circuit Model 1.Y01_03 VabcStator/Model/U A: |
| Voltage Phase B | Measurements | Circuit Model 1.Y01_03 VabcStator/Model/U B: |
| Voltage Phase C | Measurements | Circuit Model 1.Y01_03 VabcStator/Model/U C: |

3. Navigate to the **Sources** configuration page.
4. Map the **Current Phase A** and **Current Phase B** outputs of the machine model to the corresponding current sources in the circuit model.



| | Type | Group | Element |
|------------|----------------|----------------|--------------------------------|
| U01 Va | Voltage source | Sinewaves | Circuit Model 1.SWG00 |
| U02 Vb | Voltage source | Sinewaves | Circuit Model 1.SWG01 |
| U03 Vc | Voltage source | Sinewaves | Circuit Model 1.SWG02 |
| U04 IaPMSM | Current source | Dual PMSM BLDC | PMSM VDQ 1.Current Phase A (A) |
| U05 IbPMSM | Current source | Dual PMSM BLDC | PMSM VDQ 1.Current Phase B (A) |

Tuning the Snubber Values

An RC snubber is often used to stabilize the decoupling of two solvers on the FPGA (e.g. eHS solver & a machine). Ideal snubber values can be calculated based on the following parameters of the simulation:

- Nominal speed of the machine being simulated
- Power rating of the machine between simulated

For details on how to select a snubber value for your simulation, please contact [OPAL-RT Technical Support](#).