Circuit Model Section

Circuit Model Configuration Page

In the **System Explorer** window configuration tree, expand the **Power Electronics Add-On** custom device and select a **Circuit Model** section to display this page. Use this page to add an electrical model to the VeriStand System Definition. When the VeriStand project is deployed, the circuit model is simulated on the FPGA through the **eHS Solver**.

This page includes the following components:

Name	Specifies the name of the circuit model.
Description	Specifies a description for the circuit model.
Circuit Model File Path	Specifies the path to the circuit model file on disk. When a file path is added or modified, the model file is parsed and VeriStand channels are created corresponding to the **Source**, **Switch**, and **Measurement** components defined in the circuit model. Component configuration settings are set to their default states.
Reload	Parses the currently specified circuit model and updates the VeriStand channels. Components whose names have not changed retain their previously configured settings, while new or modified components are reset to the default state. Components that are no longer part of the model are removed.
Clear	Removes the currently loaded circuit model. When a circuit model is cleared, the corresponding **Source**, **Switch**, and **Measurement** sections are deleted from the Configuration Tree and all related mapping configuration settings are removed.
Timestep (s)	Specifies the Timestep of the circuit model. A value of 0 means the model will execute at the speed of the **Minimum Timestep (s)**.
Form Factor	Specifies the **form factor** of the eHS Solver that will be used to simulate the circuit model. The form factor is dependent on the selected **Hardware Configuration**.
Circuit Model File Warning	If the file at **Circuit Model File Path** has been modified on disk since the circuit model was last loaded, the following warning message is displayed: *Circuit model file has been modified on disk.* Click **Reload** to ensure that the currently loaded model is up to date with the version on disk. Reloading the model clears the warning message.
	These components are disabled until a circuit model has been loaded. Microsoft Excel is required to use the **Scenarios** feature.
Scenarios File Path	Specifies the path to the Scenarios file on disk.
New	Creates a new Scenario template file with the name and path specified in Scenarios File Path. The specified file must have the extension *.xls*.
Use Scenarios?	Enables the **Scenarios** feature in eHS. When enabled, the **Scenario ID** channel is added to the Configuration Tree.
Minimum Timestep (s)	Displays the smallest timestep at which the eHS Solver can simulate the circuit model. eHS will run the simulation at this timestep by default, unless a larger timestep is specified in the **Timestep (s)** field.
Number of Scenarios Used	Displays the number of Scenarios defined in the currently loaded Scenarios file.
Maximum Number of Scenarios	Displays the maximum number of scenarios that can be configured in the Scenarios file.
Refresh	Reanalyzes the circuit model file to refresh the information displayed under **Model Information**.

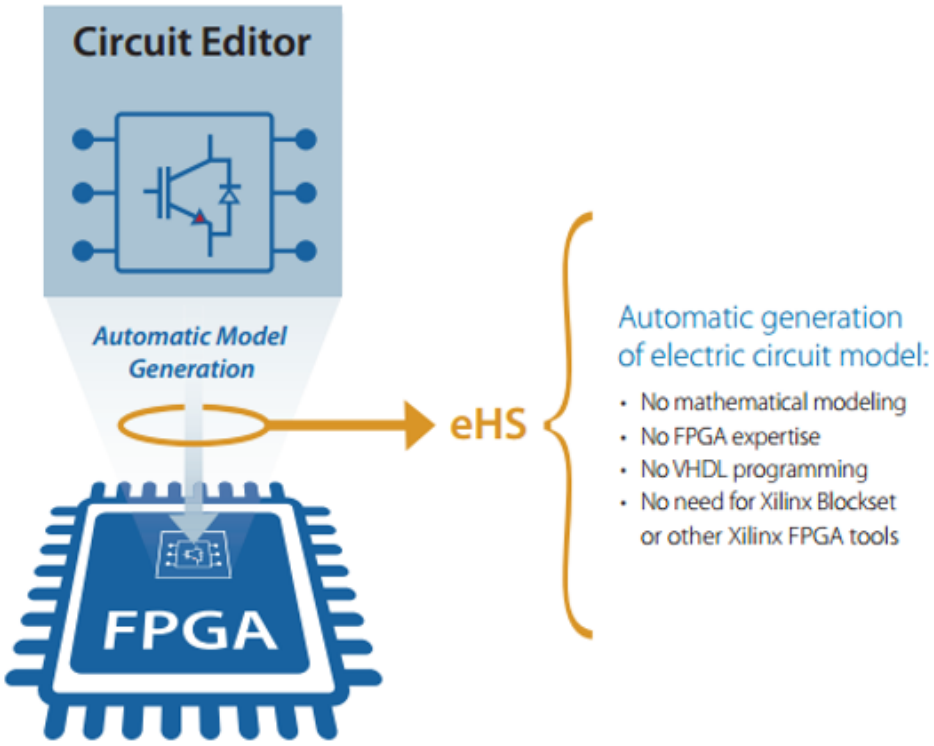
Circuit Model Section Channels

This section includes the following custom device channels:

Channel Name	Type	Default Value	Description
Scenario ID	Input	0	Specifies the index of the scenario to be simulated. Modify the value of this channel at run-time to switch between scenarios. This channel is only available when **Use Scenarios?** is enabled.

eHS Solver Description

The OPAL-RT electric Hardware Solver (eHS) is a floating-point solver that enables users to simulate an electric circuit on an FPGA without having to write the mathematical equations. It combines the simplicity of building electric circuit models using circuit editing software with the strength of FPGA-based simulators to solve the currents and voltages within the circuit in real-time, with a sample time below 1µs.



The **eHS Solver** uses **Modified Nodal Analysis** to generate a conductance matrix that, when solved, returns the voltage at each node of the circuit and the current in each branch. The conductance matrix of the circuit is generated independently from the state of the switches, and therefore does not need to be recomputed when a switch is opened or closed during the simulation. This is achieved through the implementation of the Pejovic method, which represents each **Switch** component as an impedance–a conducting switch is represented as an inductor and an open switch is represented as a capacitor.

The components within an electric circuit model can be classified into four different types, listed below. See **How to Create a Circuit Model** for more information regarding the requirements of the circuit model file.

- **Sources**
- **Switches**
- **Measurements**
- **Passive Elements**

OPAL-RT offers several different types of eHS form factors. Each form factor provides different capabilities for the number of Sources, Switches, Measurements, and Passive Elements that can be simulated.

Features	eHSx16	eHSx32	eHSx64	eHS128
Number of Sources	16	32	64	128
Number of Switches	24	48	72	144
Number of Measurements	16	32	64	128
Number of Resistors	Unlimited			
LCA capability*	Yes			

Maximum number of states**	84	112	168	344
Switches type supported	IGBT/Diode, Diode, Breaker, Thyristor, Ideal Switch			
Non-switching devices supported	Resistor, Inductor, Capacitor, Ideal Transformer, Mutual inductance, PI Line			
Calculation power (GFLOPS)	6.4	12.8	25.6	51.2
Maximum number of test scenarios***	Up to 512 scenarios			

* LCA stands for Loss Compensation Algorithm. This feature optimizes losses for standard topologies such as 2-level converter and NPC 3-level converter arms.
** Estimated values. The maximum number of states depends on the number of inputs and outputs that needs to be computed as well. There is no hard coded limit.
*** The number of scenario available for a given circuit depends on the circuit complexity

eHS Circuit Loading Behavior

Mapping and configurations settings applied to the **Source**, **Switch**, **Waveform**, and **IO** pages are preserved by saving the System Definition file. In certain cases, such as when loading a new circuit model file, these parameters may be reset to their default values.

The following actions cause the **Source** and **Switch** configuration settings to be reset to their default state:

- Renaming the circuit model file on disk and loading the file.
- Moving the circuit model file on disk and loading it from the new path.

In the following situations, all existing mappings and configuration settings are preserved (**Sources**, **Switches**, **Waveforms**, **Analog Outputs**, and **Digital Outputs**):

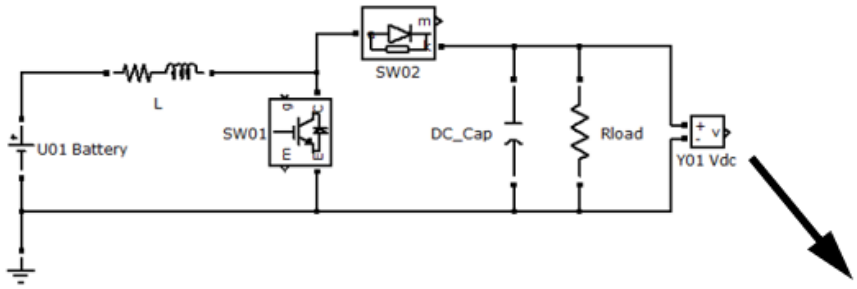
- The circuit model file is unchanged and reloaded, either by browsing to the same **Circuit Model File Path**, or by clicking the **Reload** button.
- Sources, Switches, or Measurements are added or removed, then the circuit model file is reloaded. Note that Source and Switch component mappings are only preserved for components whose names have not changed.
- Changes are made to the Passive Elements, then the circuit model file is reloaded.

Scenarios Feature Description

A Scenario is a version of the circuit model that has its own parameter settings for any **passive element** in the model. The Scenarios feature makes it possible to have multiple versions of the circuit model stored in the FPGA solver core. As the simulation is running, users can modify the value of the **Scenario ID** channel to switch from one Scenario to another and modify the model behavior. For example, this feature can be used to apply short or open circuit faults.

The Scenarios are managed inside an XLS file. A row is defined for each Scenario, while the passive components are each assigned a column in the spreadsheet. For a given Scenario, it is possible to modify as many component values as required. At execution time, users can switch between Scenarios by manipulating the value of the **Scenario ID** channel.

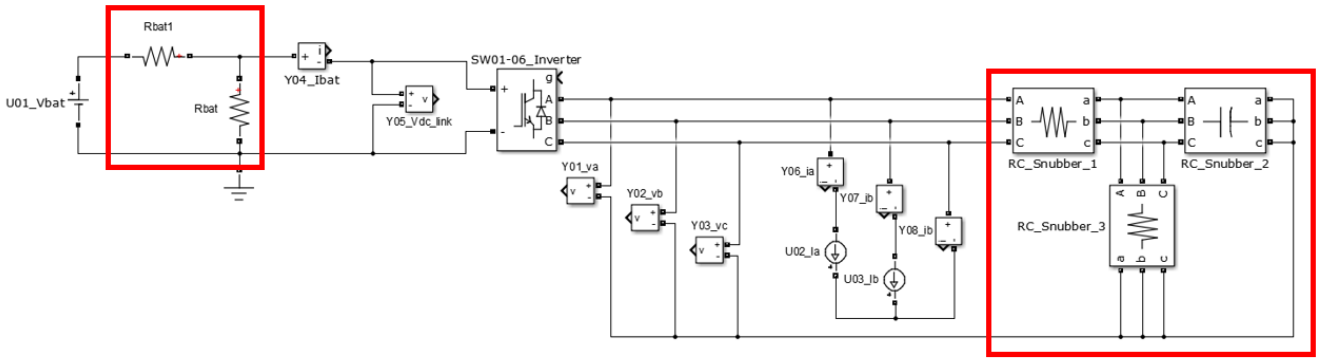
For a step by step guide to setting up Scenarios and generating the XLS Scenarios file, refer to **How To Use the Scenarios Feature**.



	A	B	C	D	E	F	G	H	I
1		DC_Cap	Rload	L.R	L.L	snubber: SW02	snubber: SW01	SW02_Ron	SW01_Ron
2	Default	0.001	10	0.02	0.001	100000	100000	0.001	0.001
3	Scenario1				0.002				
4	Scenario2	0.002							
5	Scenario3	0.002			0.002				
6	Scenario4		1						
7	Scenario5							1.00E+05	
8	Scenario6								
9	Scenario7								
10	Scenario8								
11	Scenario9								
12	Scenario10								
13	Scenario11								

Passive Elements Description

Passive elements are circuit model components such as resistors, inductors, and capacitors. Their properties cannot be changed or or updated during the simulation unless the **Scenarios** feature has been enabled. See **Supported Circuit Editors** for a list of supported passive elements in the circuit model.



Related Links

How to Create a Circuit Model

How to Add a Circuit Model to the System Definition

How to Use the Scenarios Feature