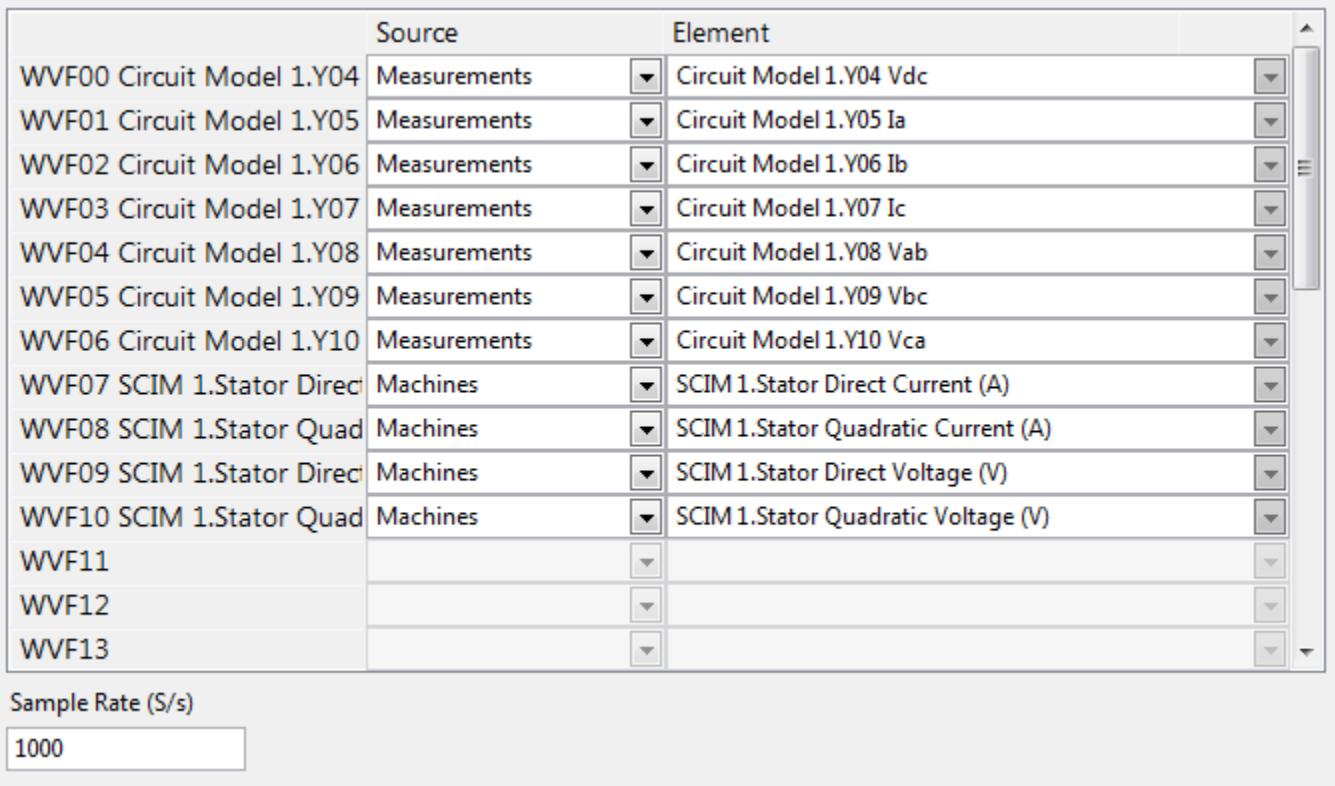
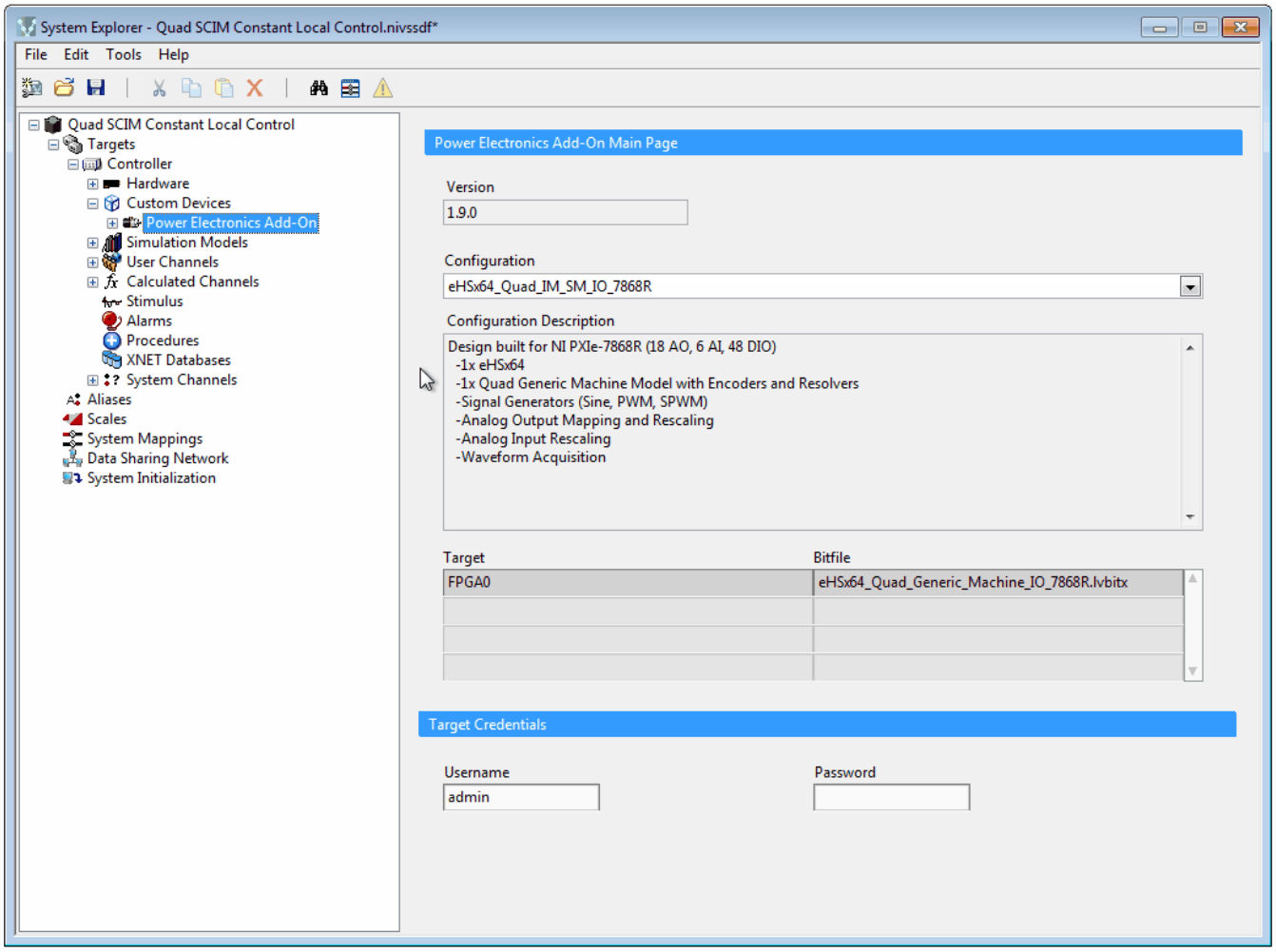
5.7 Configuring the Waveforms of the Simulation

In our user interface, we would like to display some of the signals and measurements generated on the FPGA during the simulation. To stream signals from the FPGA at a rate faster than that of the CPU execution, we can assign certain VeriStand channels to the **Waveform Acquisition** engines.

- In the Configuration Tree, expand **Circuit Model** >> **Waveforms**. Notice that 32 Waveform channels are available to be mapped to different signal sources.
- Click **Waveforms** to open the configuration page.
- Map VeriStand Channel signals to the Waveform channels as shown below. The data from these channels will be streamed at the **Sample Rate (S/s)** specified at the bottom of the window.
- Click **Save**.




System Explorer - Quad SCIM Constant Local Control.nivssdf*
File Edit Tools Help
Quad SCIM Constant Local Control
Targets
Controller
Hardware
Custom Devices
Power Electronics Add-On
Simulation Models
User Channels
Calculated Channels
Stimulus
Alarms
Procedures
XNET Databases
System Channels
Aliases
Scales
System Mappings
Data Sharing Network
System Initialization
Power Electronics Add-On Main Page
Version
1.9.0
Configuration
eHSx64_Quad_IM_SM_IO_7868R
Configuration Description
Design built for NI PXIe-7868R (18 AO, 6 AI, 48 DIO)
-1x eHSx64
-1x Quad Generic Machine Model with Encoders and Resolvers
-Signal Generators (Sine, PWM, SPWM)
-Analog Output Mapping and Rescaling
-Analog Input Rescaling
-Waveform Acquisition
Target
Bitfile
FPGA0
eHSx64_Quad_Generic_Machine_IO_7868R.lvbitx
Target Credentials
Username
admin
Password