4.7 Configuring the Waveforms of the Simulation

In our user interface, we would like to display some of the signals and measurements generated on the FPGA during the simulation. To stream signals from the FPGA at a rate faster than that of the CPU execution, we can assign certain VeriStand channels to the **Waveform Acquisition** engines.

- In the Configuration Tree, expand **Circuit Model** >> **Waveforms**. Notice that 32 Waveform channels are available to be mapped to different signal sources.
- Click **Waveforms** to open the configuration page.
- Map VeriStand Channel signals to the Waveform channels as shown below. The data from these channels will be streamed at the **Sample Rate (S/s)** specified at the bottom of the window.
- Click **Save**.

	Source	Element
WVF00 Circuit Model 1.Y01	Measurements	Circuit Model 1.Y01_03 VabcStator/Model/U A:
WVF01 Circuit Model 1.Y01	Measurements	Circuit Model 1.Y01_03 VabcStator/Model/U B:
WVF02 Circuit Model 1.Y01	Measurements	Circuit Model 1.Y01_03 VabcStator/Model/U C:
WVF03 Circuit Model 1.Y04	Measurements	Circuit Model 1.Y04 Vdc
WVF04 PMSM SH 1.Current	Dual PMSM SH	PMSM SH 1.Current Phase A (A)
WVF05 PMSM SH 1.Current	Dual PMSM SH	PMSM SH 1.Current Phase B (A)
WVF06 PMSM SH 1.Current	Dual PMSM SH	PMSM SH 1.Current Phase C (A)
WVF07 PMSM SH 1.Direct S	Dual PMSM SH	PMSM SH 1.Direct Stator Current (id0) (A)
WVF08 PMSM SH 1.Quadra	Dual PMSM SH	PMSM SH 1.Quadratic Stator Current (iq0) (A)