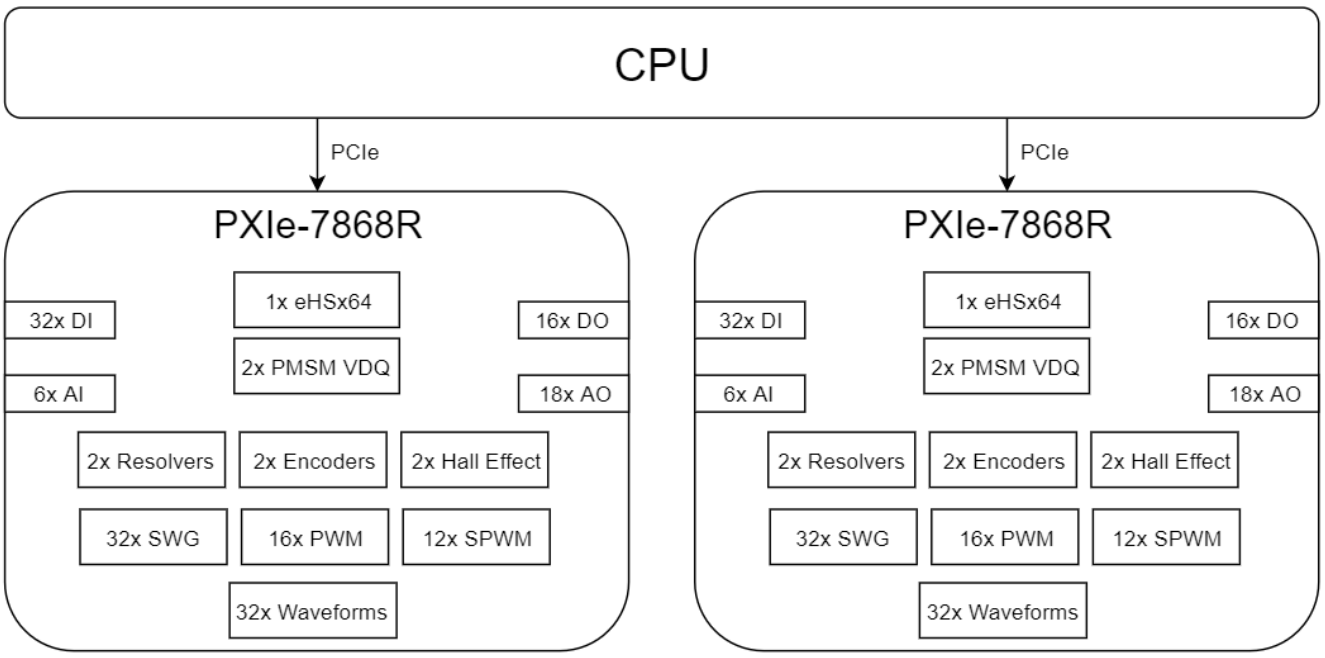
(Archived) Dual_eHSx64_Quad_PMSM_VDQ_IO_Dual_7868R

This Hardware Configuration has been archived and should not be used in new projects. Please contact **OPAL-RT Support** for more information.

In order to recreate the following configuration, please see the steps on **How to Duplicate an Existing Hardware Configuration**.

Specifications



IO Capabilities

This configuration requires the following FPGA boards. Please refer to the linked product page for additional information.

Quantity	FPGA Board
2	PXIe-7868R

Each PXIe-7868R supports the following features:

IO Type	Details
Analog Input	6 CH, 1MS\s, 16-bit, +/- 10V Input Signal Range, Differential Tunable Gain, Offset, and Min/Max Saturation
Analog Output	18 CH, 1MS\s, 16-bit User-defined mapping to Analog Outputs available with tunable Gain, Offset, and Min/Max Saturation. • Measurements • Sinewaves • CPU (VeriStand) • 2x PMSM VDQ
Digital Input	32 CH, 80MHz, 3.3V TTL (Connector 1)

Digital Output	16, 10MHz, 3.3V TTL (Connector 0) User-defined mapping to Digital Outputs available with tunable Polarity. • CPU (VeriStand) • Encoders • Hall Effect • PWMs • Digital Inputs

Refer to **7868 IO Assignation [Dual_eHSx64_Quad_PMSM_VDQ_IO_Dual_7868R]** to see the IO assignment.

Modeling Capabilities

This configuration includes a pre-compiled firmware/bitfile which is deployed to both PXIe-7868R FPGA boards. Both boards support the following features:

Features	Additional Information
1x eHSx64 Solver	User-defined mapping to Circuit Sources available: • CPU (VeriStand) • Sinewaves • Dual PMSM VDQ • Analog Inputs User-defined mapping to Circuit Switches available: • CPU (VeriStand) • PWMs • SPWMs • Digital Inputs
2x PMSM Variable Parameter Solver	Each machine supports two modes: Constant Parameter and Variable Parameter. In constant parameter mode, Ld, Lq, and flux is constant. In variable parameter mode, a user can configure the solver to such that Ld, Lq, and flux varies according to Id and Iq. Refer to the **PMSM BLDC Section** for more information.
1x Resolver/motor	Excitation assignable to any analog input port
1x Encoder/motor	Assignable to any DO port
1x Hall Effect Sensor/motor	Assignable to any DO port
32x Sinewave Generators	
16x PWM Generators	
12x Sinusoidal PWM Generators	
Analog Output Mapping and Rescaling	
Analog Input Rescaling	
32x Waveform Acquisition Channels	

The two PXIe-7868R cards are not configured to communicate with each other via peer-to-peer streams and are therefore running completely independently from one another. However, they can be interconnected at the RT CPU level using VeriStand channels.