OP5700 IO Configuration

The OP5700 simulator provides signal conditioning for up to 256 I/Os, which are managed from the FPGA module and are accessible via DB37 and RJ45 connectors in the back and front of the chassis.

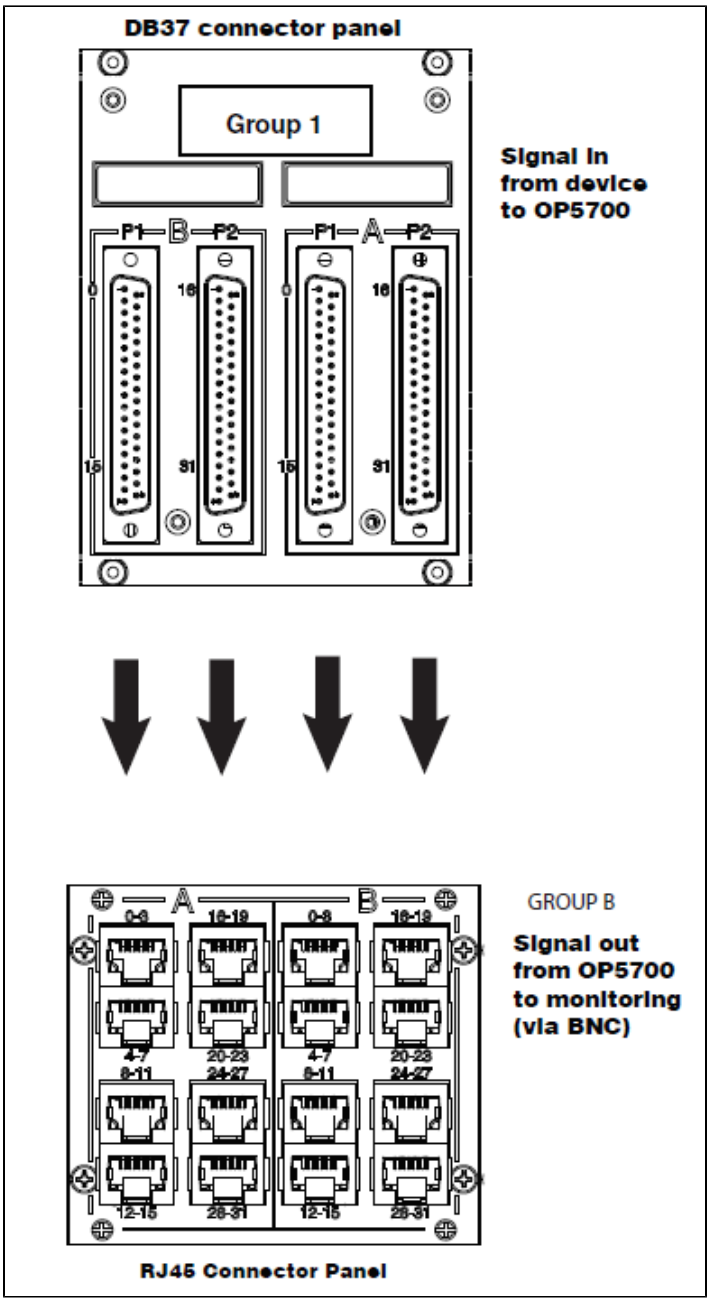
I/O lines are routed through a carrier board (inside the chassis) that can accept up to 8 signal conditioning modules, which provides greater signal conditioning flexibility. The conditioning modules follow a proprietary form factor, called Type B mezzanines. A range of mezzanines is available for analog and digital conditioning.

Mezzanines are detected at power-up and information is processed by the FPGA for verification and initialization (I/O line direction, analog module calibration coefficients, etc.). Then, mezzanines are made available to the CPU simulation to detect improper configuration or hardware failure.

DB37 Connectors

There are 4 groups of mezzanines, labeled 1 to 4; each pair (A & B) is linked to four female DB37 connectors (I/Os) on the back of the chassis:

The first two connectors (left to right) represent channels from Group B, which are linked to the conditioned channels from the rear mezzanine. The last two connectors (left to right) represent channels from Group A, which are linked to the conditioned channels from the front mezzanine.



Two DB37F connectors (P1 and P2) are available for each mezzanine, and their pinout depends on the type of mezzanine installed:

Analog modules (DAC or ADC), which use only 16 channels, which are routed through connector P1 and P2 do not carry any signals.

Digital modules (Din or Dout), which use up to 32 channels; the first 16 channels (00 to 15) are routed through connector P1 and the next 16 channels (16 to 31) are routed through connector P2.

All signals are represented by a positive-negative pair that are always available on the connector pins, for example: for channel 08 : (+CH08, -CH08).

Connector Interface:

Single-ended output	Negative pin is connected to ground
Single-ended input	User's ground must be connected to the negative pin
Differential output	Positive and negative signals must be on positive and negative pins
Differential input	Connection must be between the positive/negative pair