OP5650 System Description

The OP5650 is a complete simulation system, that contains a powerful target computer, a reconfigurable FPGA and signal conditioning for up to 256 I/Os. The design makes it easy to use with standard connectors (DB37, RJ45, SFP, and mini-BNC) without the need for input/output adaptors and allows quick connections for monitoring I/O signals. It is designed to be used either as a desktop, shelf top, or mounted in a standard 19'' rack.

Simulator Architecture

The front of the chassis provides access to the target computer's standard connectors, and monitoring interfaces and connectors, while the back of the chassis provides access to the I/O connectors, power cable and main power switch.

The main housing is divided into two sections, each with a specific purpose:

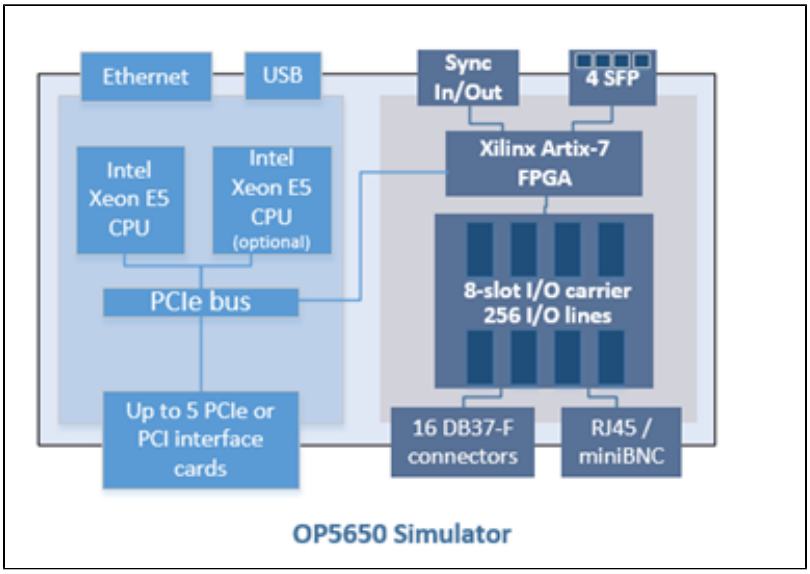
The **lower section** of the chassis contains a powerful target computer that can be added to a network of simulators or can act as a standalone. The target computer is used to run simulations built with OPAL-RT's RT-LAB or HYPERSIM software simulation platform and includes the following features:

- ATX motherboard
- Linux-based real-time operating system
- Xeon E5 Intel CPU with 4, 8, 16 and 32 processor cores, CPU frequency between 2.3 and 3.2GHz, and 10MB Cache Memory per 4 cores. See C onfiguration Options below for more details.
- up to 32GB of DRAM
- 512GB SSD disk,
- Space to install 2 PCI with risers, or 3 PCIe
- Power consumption: 600W

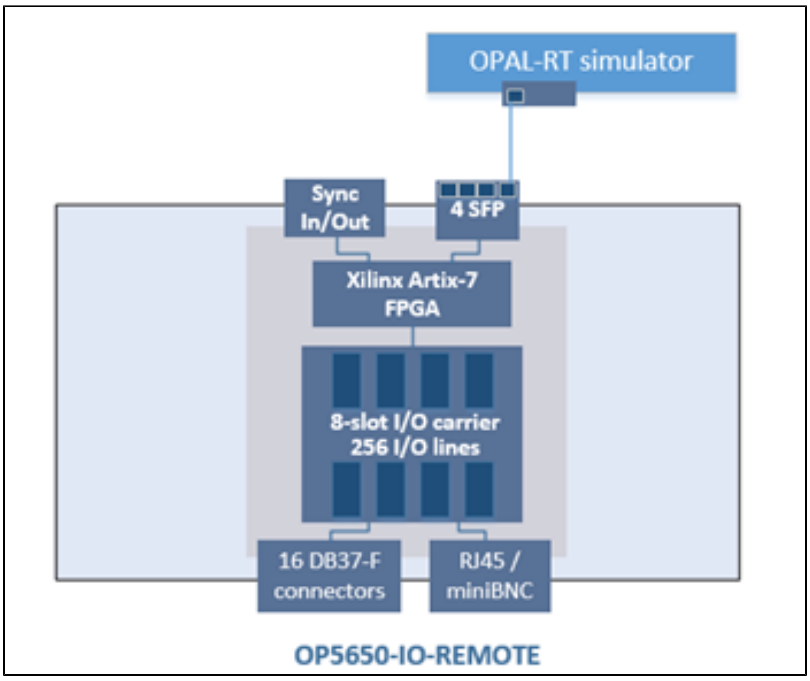
The **upper section** contains the high-speed FPGA and the conditioning modules for up to 256 I/Os. It includes:

- A Xilinx Artix-7 FPGA 200T installed on OPAL-RT OP5143 board, programmable from the target computer via PCIe or MUlti-System Expansion (MuSE). The FPGA is used to execute models designed with the OPAL-RT RT-XSG tool and manage the I/O lines. It exchanges data with the real-time simulations running on the target computer CPUs via PCIe.
- An 8-slot fat carrier capable of connecting any combination of up to 8 OP5300 mezzanine modules.

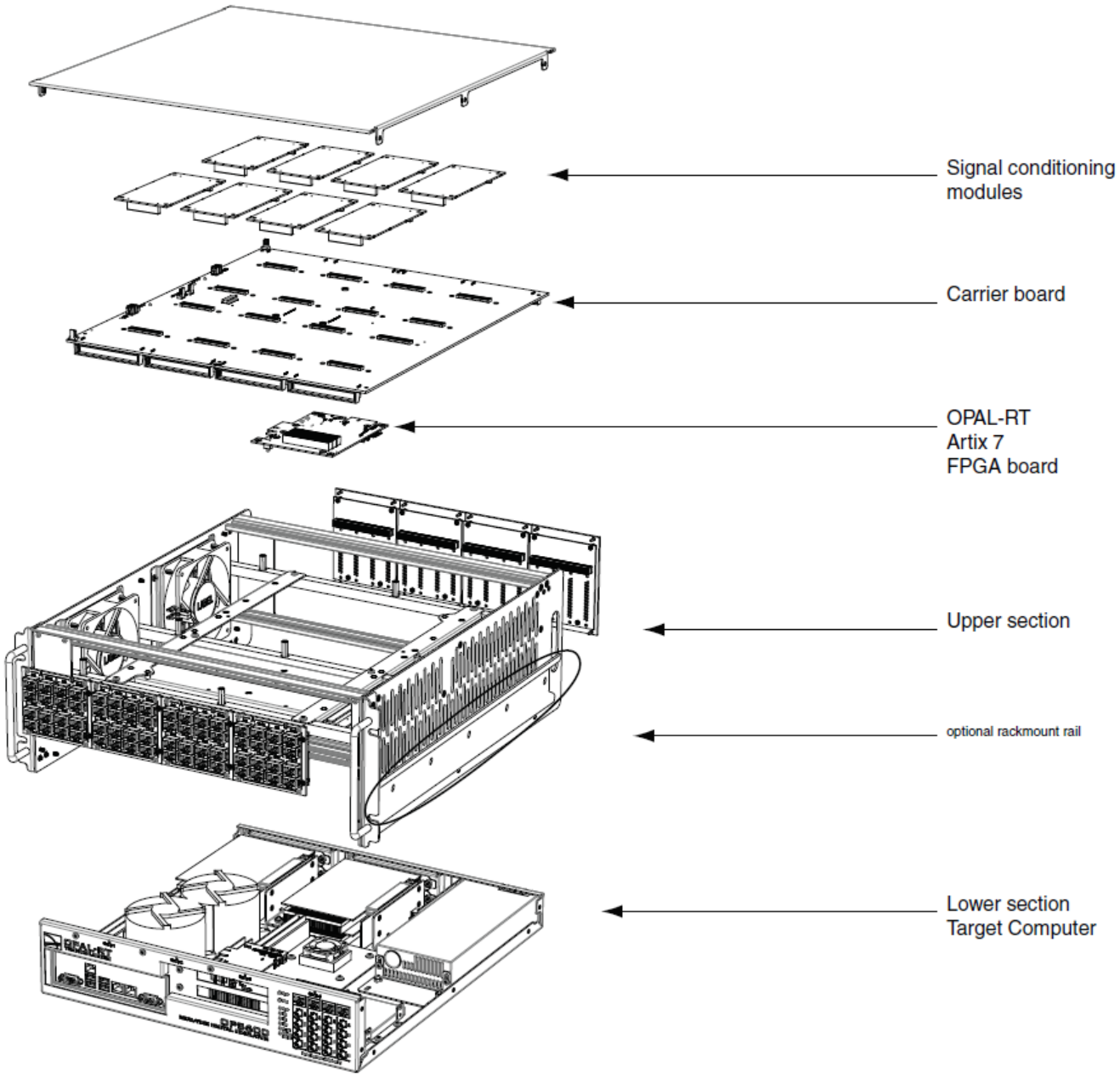
These features can be represented by the diagram below :



The OP5650 also comes as an I/O expansion unit, the OP5650-IO-REMOTE, which connects via OPAL-RT MUlti-System Expansion (MuSE) link to a real-time simulator.



The figure below represents the chassis structure in 3D :



Note: The example shown is only to illustrate how the OP5650 is assembled. OPAL-RT strictly prohibits users from opening the OP5650. Opening the unit renders the warranty null and void.

Configuration Options

The OP5650 is available in a number of different configurations that make it easier to integrate into your environment:

Product	Configuration Description

OP5650-4	OP5650 RCP/HIL Artix 7 FPGA-based Real-Time Simulator - 4 cores (4U, Xeon E5, 4 Cores, 3.0 GHz, 10M, 16GB, 512GB SSD)
OP5650-8	OP5650 RCP/HIL Artix 7 FPGA-based Real-Time Simulator - 8 cores (4U, Xeon E5, 8 Cores, 3.2 GHz, 20M, 16GB, 512GB SSD)
OP5650-16	OP5650 RCP/HIL Artix 7 FPGA-based Real-Time Simulator - 16 cores (4U, Xeon E5, 2x8 Cores, 3.2 GHz, 2x20M, 2x16GB, 512GB SSD)
OP5650-32	OP5650 RCP/HIL Artix 7 FPGA-based Real-Time Simulator - 32 cores (4U, Xeon E5, 2x16 Cores, 2.3 GHz, 2x40M, 2x16GB, 512GB SSD)