OP5700 System Description

The OP5700 is a complete simulation system. It contains a powerful target computer, a high-end reconfigurable FPGA, signal conditioning for up to 256 I/O lines and 16 high-speed fiber-optic SFP ports. The design makes it easy to use with standard connectors (DB37, RJ45, and mini-BNC) without the need for input/output adaptors and allows quick connections for monitoring I/O signals.

It is designed to be used either as a desktop, shelf top, or mounted in a standard 19'' rack. The front of the chassis provides access to monitoring interfaces and connectors and the SFP sockets, while the back of the chassis provides access to the target computer's standard connectors, I/O connectors, power cable, and main power switch.

System architecture

The main housing is divided into two sections, each with a specific purpose:

The **lower part** of the chassis contains the target computer that can be added to a network of simulators or can run standalone. The target computer, used to run simulations built with OPAL-RT's RT-LAB or HYPERSIM tools, includes the following features:

- ATX motherboard
- Linux-based real-time operating system
- Intel Xeon E5 CPU with 4, 8, 16 and 32 processor cores, up to 3.2GHz. See Configuration Options below.
- 10MB Cache Memory per 4 cores
- up to 32GB of DRAM
- 512GB SSD disk
- 6 PCIe slots used to connect the internal FPGA board and PCIe or PCI third-party I/O and communication cards

> **Note**
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> The CPU configuration and the use of riser boards for PCI cards may limit the number of available slots, as described in the Hardware configuration section

The **upper section** contains the FPGA and the I/O conditioning modules. It includes:

- a Xilinx Virtex 7 FPGA programmable from the target computer via PCIe. The FPGA is used to execute models designed with the OPAL-RT RT-XSG tool, manage the I/O lines and execute embedded FPGA-based simulations. It exchanges data with the real-time simulations running on the target computer CPUs via the PCIe link
- an 8-slot flat carrier board capable of connecting any combination of up to 8 digital and analog conditioning modules. Each module controls 16 or 32 lines for a total of up to 256 I/0 lines.
- 16 SFP ports for high-speed communication with other FPGA-based systems or with external devices. The standard communication protocols available with the OP5707 are based on Xilinx Aurora (1 to 5 Gbps). Other protocols, such as the Gigabit Ethernet, can also be implemented. These SFP ports can be used to expand the simulator's I/O capability using OPAL-RT's **MUlti-System Expansion link (MuSE)**: each port can be connected to one OPAL-RT remote I/O unit (OP4520, OP5607 or OP4200), effectively increasing the simulator I/O capability to a maximum of 4096 channels. SFP ports not used for MuSE remain compatible with the legacy Generic Aurora link. The MuSE link is compatible with OPAL-RT boards I/O management architecture.

> **Note**
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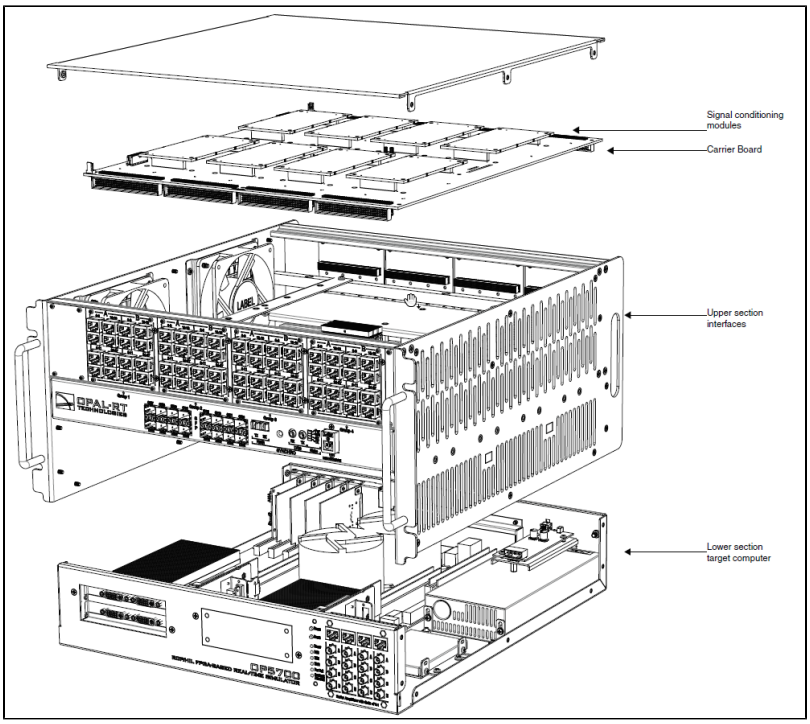
> **Note:** Restrictions to using MuSE with OPAL-RT board software architecture may apply depending on your application and software configuration. Contact your sales representative or field application engineer to verify compatibility

The figure below illustrates this architecture.



The image shown above is used to **illustrate** the layered and flexible product architecture.
Customers should not open the chassis unless under the strict guidance of Technical Support.
To do so may **invalidate your warranty**.

Configuration Options

The OP5700 is available in a number of CPU configurations that are factory configured according to the customer's processing requirement.

Product	Configuration Description
OP5707-4	OP5700 RCP/HIL Virtex7 FPGA-based Real-Time Simulator - 4 cores (5U, Xeon E5, 4 Cores, 3.0 GHz, 10M, 16GB, 512GB SSD)
OP5707-8	OP5700 RCP/HIL Virtex7 FPGA-based Real-Time Simulator - 8 cores (5U, Xeon E5, 8 Cores, 3.2 GHz, 20M, 16GB, 512GB SSD)
OP5707-16	OP5700 RCP/HIL Virtex7 FPGA-based Real-Time Simulator - 16 cores (5U, Xeon E5, 2x8 Cores, 3.2 GHz, 2x20M, 2x16GB, 512GB SSD)
OP5707-32	OP5700 RCP/HIL Virtex7 FPGA-based Real-Time Simulator - 32 cores (5U, Xeon E5, 2x16 Cores, 2.3 GHz, 2x40M, 2x16GB, 512GB SSD)

Note

The OP5700 is built with the same FPGA and I/O architecture as the OP5607 I/O expansion chassis (OP5600 family of products), therefore the FPGA programming files (bitstreams) are fully compatible.

System Interconnection Details

There are two standard modes of operation available for the SFP ports, both based on the Xilinx Aurora communication protocol:

- **Generic Aurora communication:** this mode is enabled using the RT-XSG blockset's Generic Aurora blocks in the FPGA programming file's Simulink model. These blocks are used to exchange data with third-party devices or with other OPAL-RT systems The data communication layer (data packing/ unpacking) must be configured by the user according to the targeted application. The communication speed is configurable between 1 and 5 Gbps and the SFP transceivers should be selected accordingly.
- **MUlti-System Expansion link (MuSE):** this mode encapsulates the Aurora protocol within a network protocol designed by OPAL-RT for inter-system communication. The communication speed is set to 5Gbps by default, but downgrades automatically to the speed of the other port, if that port is used at a lower speed for third-party device connection.

The MuSE mode is selected in the RT-XSG block by setting the synthesis manager architecture option to **<remote>.** In this mode, the unit must be connected to another OPAL-RT system that is connected in central mode, and it then becomes a remote expansion unit (similar to an OP4520 or OP4200).