PDL Inputs specifications

The PDL module has three types of channels for monitoring input signals: Standard, Bipolar and Flexible. The specifications of each type are described below.

The inputs' analog and digital states are continuously monitored to extract all transitions. Period and duty cycle are computed using the transition timestamps. A 12-bit analog to digital converter is used to measure the analog state.

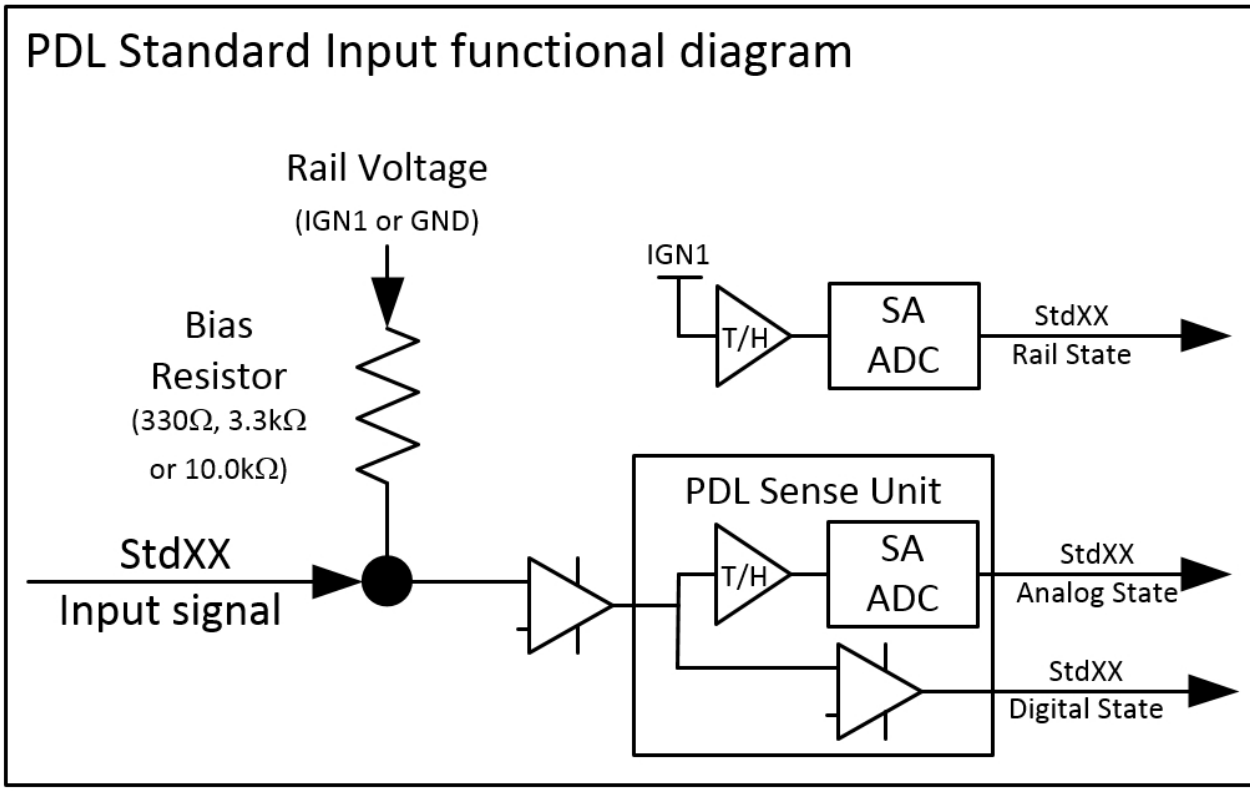
Each input operating voltage is 0 to 16 V and the sense unit impedance is superior to 100K. All inputs are tolerant from –1 V to 27 V.

Standard Inputs (STD_A0:16, STD_B0:3, STD_C0:3, STD_D0:6)

The 32 standard input lines are tied to either IGN1 or GND via a bias resistor. The channels are grouped in 4 sub-types types (A, B, C and D) having different values of the bias resistor (300, 3k, 10k) and the reference state (IGN1 or GND) as follows :

Sub-type	Number of channels	Bias resistor value	Reference state
A	17	330	IGN1
B	4	330	GND
C	4	3.3 k	IGN1
D	7	10 k	IGN1

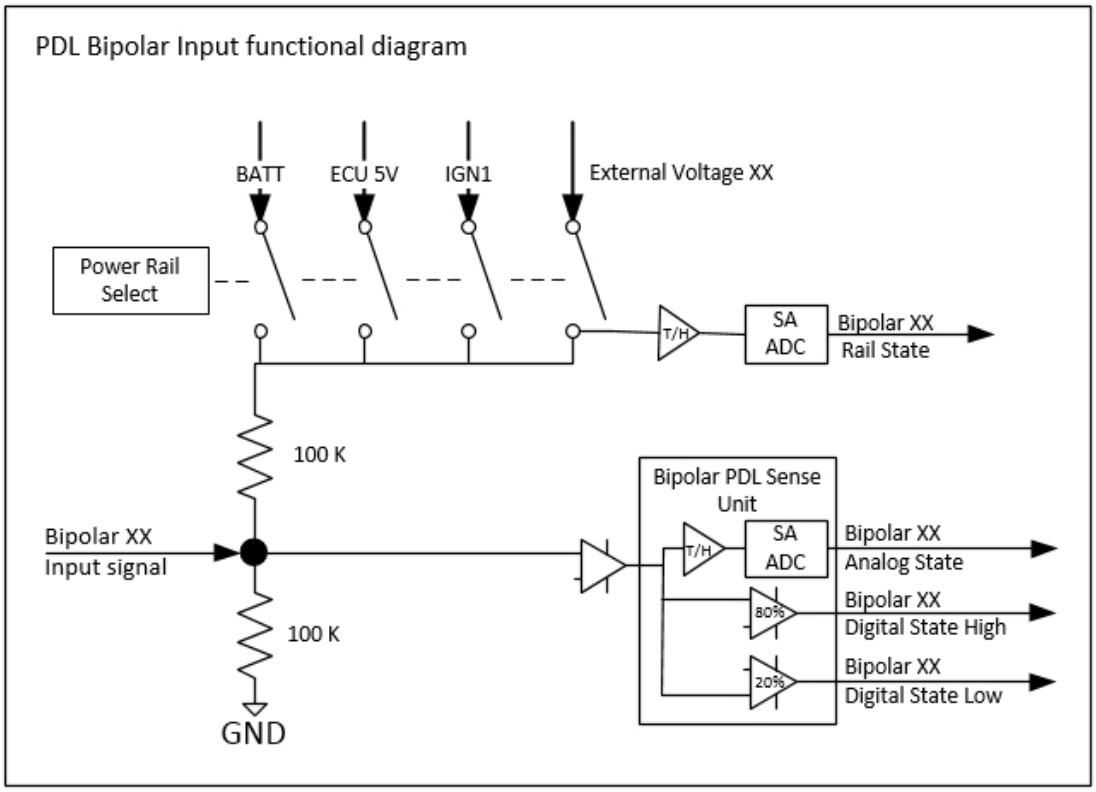
The figure below represents the electrical schematic of a standard PDL input. At the board level, the sense units report a high when the input voltage is above 3.5 V ± 10% and low when the input is below 1.5 V ± 10%. The FPGA module of the card reports all transitions occurring on the input lines during one calculation step of the model, as well as the values of the analog states.



Bipolar Inputs (BIP_[1:0] & B_EXTV[1:0])

The 2 Bipolar PDL inputs are typically used to monitor bipolar signals with a positive voltage offset. They allow selection of the power rail among BATT, ECU 5V, IGN1 or an External voltage; and a fixed bias set to 50% of the rail voltage.

The figure below represents the electrical schematic of a bipolar PDL input. It illustrates that the input is internally connected to 50% of the rail voltage via bias resistors. The sense units indicate high when the input voltage is above 80% of rail voltage and low when the input is below 20% of rail voltage.



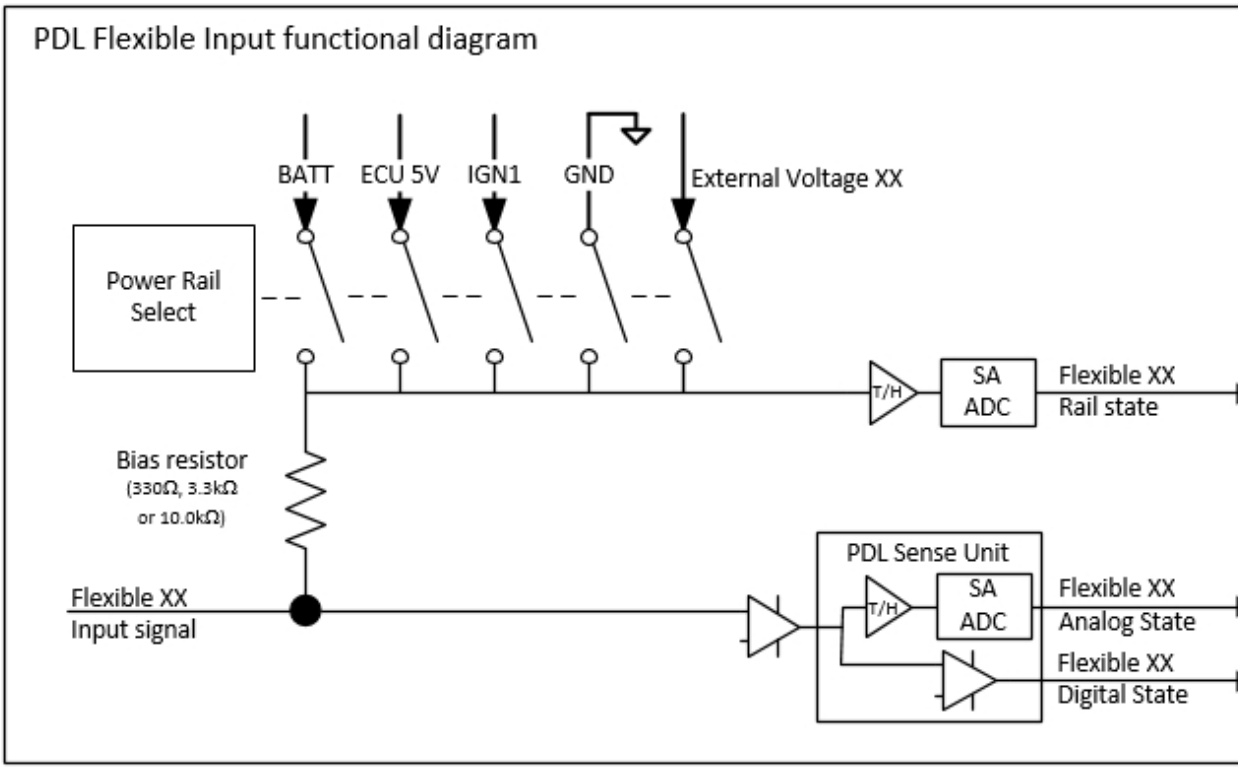
Flexible PDL Inputs (F_[4:0] & F_EXTV[4:0])

Flexible PDL inputs are typically used to monitor digital signals that are referenced to BATT, ECU5V, IGN1, GND or an external voltage.

The input signals are tied to rail via a bias resistor :

Input number	Bias resistor value
0	330
1	330
2	3.3 k
3	3.3 k
4	10 k

The figure below represents the electrical schematic of a flexible PDL input. It illustrates that the input is internally connected to the rail voltage via the bias resistor. The sense units indicate high when the input voltage is above 3.5 V ± 10% and low when the input is below 1.5 V ± 10%.


PDL Flexible Input functional diagram
BATT
ECU 5V
IGN1
GND
External Voltage XX
Power Rail Select
T/H
SA ADC
Flexible XX Rail state
Bias resistor
(330Ω, 3.3kΩ or 10.0kΩ)
PDL Sense Unit
Flexible XX Input signal
T/H
SA ADC
Flexible XX Analog State
Flexible XX Digital State